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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,218	11/25/2003	Shui-Ming Cheng	24061.149	6790

42717 7590 03/22/2006

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EXAMINER	
CAO, PHAT X	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/722,218	Applicant(s) CHENG ET AL.	
	Examiner Phat X. Cao	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 5, 8-12, and 44 are rejected under 35 U.S.C. 102(e) as being anticipated by Ouyang et al (US. 2005/0093021).

Regarding claims 1 and 44, Ouyang (Fig. 4B) discloses a method of manufacturing a semiconductor device, comprising: forming an isolation region 54 located in a substrate; forming an NMOS device located partially over a surface of the substrate 40'; and forming a PMOS device isolated from the NMOS device by the isolation region 54 and located partially over the surface 40 (par. [0040]); wherein a first one of the NMOS and PMOS devices includes the PMOS device having first source/drain regions 10 recessed within the surface 40 (par. [0040], lines 8-13); and wherein a second one of the NMOS and PMOS devices includes the NMOS device having second source/drain regions 70 substantially coplanar with the surface 40'.

Regarding claims 5 and 12, Ouyang (Fig. 4B) further discloses that the set of PMOS source/drain regions comprise strained source/drain regions 10 of SiGe (par. [0027], lines 9-17 and par. [0028]).

Regarding claims 8-9, Ouyang further discloses that the substrate has a {110} or {100} crystal orientation (par. [0029]).

Regarding claims 11 and 12, Ouyang also discloses that the substrate is a bulk silicon substrate or a silicon-on-insulator substrate (SOI) (par. [0033]).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-4, 13-14, 16-18, 21-26, 28-29, 32-36, and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al in view of Dawson et al (US. 5,963,803).

Regarding claims 2, 16 and 45, Ouyang's Fig. 4B also discloses that the magnitudes of stresses in the first and second source/drain regions are different, the difference in magnitudes of stresses are caused by the difference in structures of the first and second source/drain regions of the NMOS and PMOS devices (par. [0027]).

Ouyang does not disclose the PMOS gate having a height greater than a height of the NMOS gate.

However, Dawson (Fig. 1H) teaches a CMOS device comprising a PMOS gate 122 having a height greater than a height of an NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Ouyang by forming the PMOS gate having a height greater than a height of the NMOS gate because the

relatively high gate for the PMOS device would reduce boron penetration into active region, as taught by Dawson (column 4, lines 32-33).

Regarding claims 3-4, 17, 28 and 46, as discussed above, Ouyang's Fig. 4B substantially reads on the invention as claimed, except it does not disclose that the spacers 51 formed on opposing sides of the PMOS have a width greater than a width of the spacers 51 formed on opposing sides of the NMOS gate.

However, Dawson (Fig. 1H) teaches a CMOS comprising the spacers 146 formed on opposing sides of the PMOS gate 122 and having a width greater than a width of the spacers 144 formed on opposing sides of the NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Ouyang by forming the spacers on opposing sides of the PMOS gate having a width greater than a width of the spacers on opposing sides of the NMOS gate because the relative wide spacers for the PMOS device would offset the rapid diffusion of boron in the source/drain regions for the P-channel device during high temperature processing so that the source/drain regions for the NMOS and PMOS devices would have the desired sizes, as taught by Dawson (column 4, lines 32-40).

Regarding claims 13-14, 18, 25-26, 29, and 36, Ouyang's Fig. 4B further discloses that the set of PMOS source/drain regions comprise strained source/drain regions 10 of SiGe (par. [0027], lines 9-17 and par. [0028]).

Regarding claims 21-22, 23-24, and 32-35, Ouyang also discloses that the substrate has a {110} or {100} crystal orientation (par. [0029]) and the substrate is a bulk silicon substrate or a silicon-on-insulator substrate (SOI) (par. [0033]).

5. Claims 6-7, 38-39 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al as applied to claim 1 above, and further in view of Yeo et al (US. 2004/0173815).

Regarding claims 6-7 and 38, Ouyang's Fig. 4B discloses a semiconductor device, comprising: an isolation region 54 located in a substrate; an NMOS device located partially over a surface of the substrate 40'; and a PMOS device isolated from the NMOS device by the isolation region 54 and located partially over the surface 40; wherein the PMOS device includes first source/drain regions 10 located at least partially within the substrate 40 and comprising SiGe (par. [0040]); and wherein the NMOS device includes second source/drain regions 70 located at least partially within the substrate 40'.

Ouyang does not disclose that the NMOS source/drain regions 70 comprise SiC.

However, Yeo (Fig. 3B) teaches an NMOS device 3b having source/drain regions 304b/302b comprising silicon and lattice-mismatched zone 305b made of silicon-carbon alloy (SiC) (par. [0033]). Accordingly, it would have been obvious to modify the device of Ouyang by forming the NMOS device having source/drain regions comprising silicon and lattice-mismatched zone made of SiC because such lattice-mismatched zone of SiC would significantly enhance the electron mobility of the drive current in the strained channel region, as taught by Yeo (par. [0033], last 8 lines).

Regarding claims 39 and 42, Ouyang's Fig. 4B further discloses that the first source/drain regions 10 of the PMOS device are recessed within the surface (par. [0040]) and the second source/drain regions 70 of the NMOS device extend downward

from the surface, and the set of the first source/drain regions 10 of PMOS device comprises strained source/drain regions (par. [0027], lines 9-17 and par. [0028]).

6. Claims 40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al and Yeo et al as applied to claim 38 above, and further in view of Dawson et al (US. 5,963,803).

Regarding claim 40, Ouyang does not disclose the PMOS gate having a height greater than a height of the NMOS gate.

However, Dawson (Fig. 1H) teaches a CMOS device comprising a PMOS gate 122 having a height greater than a height of an NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Ouyang by forming the PMOS gate having a height greater than a height of the NMOS gate because the relatively high gate for the PMOS device would reduce boron penetration into active region, as taught by Dawson (column 4, lines 32-33).

Regarding claim 41, Ouyang does not disclose that the spacer 51 formed on opposing sides of the PMOS gate has a width greater than a width of the spacer 51 formed on opposing sides of the NMOS gate.

However, Dawson (Fig. 1H) teaches a CMOS comprising the spacers 146 formed on opposing sides of the PMOS gate 122 and having a width greater than a width of the spacers 144 formed on opposing sides of the NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Ouyang by forming the spacers on opposing sides of the PMOS gate having a width greater than a width of the spacers on opposing sides of the NMOS gate because the relative wide

spacers for the PMOS device would offset the rapid diffusion of boron in the source/drain regions for the P-channel device during high temperature processing so that the source/drain regions for the NMOS and PMOS devices would have the desired sizes, as taught by Dawson (column 4, lines 32-40).

7. Claims 19-20 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al and Dawson et al as applied to claim (16,28) above, and further in view of Yeo et al (US. 2004/0173815).

Ouyang does not disclose that the NMOS source/drain regions 70 comprises SiC.

However, Yeo (Fig. 3B) teaches an NMOS device 3b having source/drain regions 304b/302b comprising silicon and lattice-mismatched zone 305b made of silicon-carbon alloy (SiC) (par. [0033]). Accordingly, it would have been obvious to modify the device of Ouyang by forming the NMOS device having source/drain regions comprising silicon and lattice-mismatched zone made of SiC because such lattice-mismatched zone of SiC would significantly enhance the electron mobility of the drive current in the strained channel region, as taught by Yeo (par. [0033], last 8 lines).

8. Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al (US. 2005/0093021) in view of Okumura et al (US. 5,428,239).

Ouyang (Fig. 4B) discloses an integrated circuit device, comprising a CMOS including: an isolation region 54 located in a substrate; an NMOS device located partially over a surface of the substrate 40'; and a PMOS device isolated from the NMOS device by the isolation region 54 and located partially over the surface 40 (par.

[0040]); wherein a first one of the NMOS and PMOS devices includes the PMOS device having first source/drain regions 10 recessed within the surface 40 (par. [0040], lines 8-13); and wherein a second one of the NMOS and PMOS devices includes the NMOS device having second source/drain regions 70 substantially coplanar with the surface 40'.

Ouyang does not disclose that the integrated circuit device comprising a plurality of CMOS devices.

However, Okumura (Fig. 1) teaches the forming of a memory integrated circuit device comprising a plurality of CMOS devices. Accordingly, it would have been obvious to modify the device of Ouyang by forming a plurality of CMOS devices in order to provide a DRAM device, as taught by Okumura (see abstract). It also would have been obvious to provide a plurality of interconnects connecting ones of the plurality of CMOS devices because such interconnects connections are well known in the art for providing the electrical connections to the CMOS devices.

9. Claims 48-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al and Okumura et al as applied to claim 47 above, and further in view of Dawson et al (US. 5,963,803).

Regarding claim 48, Ouyang does not disclose the PMOS gate having a height greater than a height of the NMOS gate.

However, Dawson (Fig. 1H) teaches a CMOS device comprising a PMOS gate 122 having a height greater than a height of an NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Ouyang by forming the

PMOS gate having a height greater than a height of the NMOS gate because the relatively high gate for the PMOS device would reduce boron penetration into active region, as taught by Dawson (column 4, lines 32-33).

Regarding claim 49, Ouyang does not disclose that the spacer 51 formed on opposing sides of the PMOS gate has a width greater than a width of the spacer 51 formed on opposing sides of the NMOS gate.

However, Dawson (Fig. 1H) teaches a CMOS comprising the spacers 146 formed on opposing sides of the PMOS gate 122 and having a width greater than a width of the spacers 144 formed on opposing sides of the NMOS gate 126 (column 7, lines 4-6). Accordingly, it would have been obvious to modify the device of Ouyang by forming the spacers on opposing sides of the PMOS gate having a width greater than a width of the spacers on opposing sides of the NMOS gate because the relative wide spacers for the PMOS device would offset the rapid diffusion of boron in the source/drain regions for the P-channel device during high temperature processing so that the source/drain regions for the NMOS and PMOS devices would have the desired sizes, as taught by Dawson (column 4, lines 32-40).

10. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al in view of Shimizu (IEEE).

Ouyang does not disclose an etch stop layer over the CMOS device and imparting the different stresses in the source/drain regions of NMOS and PMOS devices.

However, Shimizu (Fig. 1) teaches the forming of an etch stop layer of SiN over the CMOS device and imparting the different stresses in the source/drain regions of NMOS and PMOS devices (see first two pages). Accordingly, it would have been obvious to form over the NMOS and PMOS devices of Ouyang with the etch stop structure as set forth above in order to improve the drive currents for both NMOS and PMOS devices, as taught by Shimizu (see abstract).

11. Claims 27 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al and Dawson et al as applied to claim (16,28) above, and further in view of Shimizu et al (IEEE).

Ouyang does not disclose an etch stop layer over the CMOS device and imparting the different stresses in the source/drain regions of NMOS and PMOS devices.

However, Shimizu (Fig. 1) teaches the forming of an etch stop layer of SiN over the CMOS device and imparting the different stresses in the source/drain regions of NMOS and PMOS devices (see first two pages). Accordingly, it would have been obvious to form over the NMOS and PMOS devices of Ouyang with the etch stop structure as set forth above in order to improve the drive currents for both NMOS and PMOS devices, as taught by Shimizu (see abstract).

12. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al and Yeo et al as applied to claim 38 above, and further in view of Shimizu et al (IEEE).

Ouyang does not disclose an etch stop layer over the CMOS device and

imparting the different stresses in the source/drain regions of NMOS and PMOS devices.

However, Shimizu (Fig. 1) teaches the forming of an etch stop layer of SiN over the CMOS device and imparting the different stresses in the source/drain regions of NMOS and PMOS devices (see first two pages). Accordingly, it would have been obvious to form over the NMOS and PMOS devices of Ouyang with the etch stop structure as set forth above in order to improve the drive currents for both NMOS and PMOS devices, as taught by Shimizu (see abstract).

Response to Arguments

13. Applicant's arguments filed 1/6/06 have been fully considered but they are not persuasive.

Rejections under 35 U.S.C. 102(e): Claims 1, 5, 8-12 and 44 as being anticipated by Ouyang et al.

Applicant argues that Ouyang's Fig. 4B does not suggest that a PMOS includes "source/drain regions recessed within the surface", and an NMOS includes "source/drain regions substantially coplanar with the surface" as claimed.

This argument is not persuasive. The examiner recognizes that one skilled in the art would have no difficulty to recognize that the PMOS device shown in Fig. 4B of Ouyang would have source/drain regions 10 recessed within the surface of the substrate 40. Specifically, Ouyang clearly discloses that the recessed source/drain regions 10 of PMOS shown in Fig. 4B are formed by the same processes carried out shown in Fig. 3 (par. [0040], lines 8-13). The recesses source/drain regions 10 are

formed by first forming recesses within the surface of the substrate 40 (see Fig. 3C, and par. [0035], lines 8-12), and then depositing "P-doped SiGe alloy into **the recessed source/drain regions**" (see Fig. 3D and par. [0036], lines 1-2). Furthermore, Ouyang also states at par. [0040], lines 8-13 that:

"Fig. 4A shows the devices at an intermediate state of processing with all steps before the source/drain recession carried out as shown in Fig. 3 ... However, **the source/drain recessing** and SiGe source/drain epi steps **are performed only for the PMOS**."

Therefore, Fig. 4B of Ouyang clearly discloses a PMOS including "source/drain regions recessed within the surface" of the substrate.

The examiner also recognizes that one skilled in the art would also have no difficulty to recognize that the NMOS device shown in Fig. 4B of Ouyang would have source/drain regions substantially coplanar with the surface of the substrate because source/drain regions 70 of NMOS device clearly having <u>top surfaces</u> substantially coplanar with the surface of the substrate 40'. Thus, Fig. 4B of Ouyang clearly discloses an NMOS including "source/drain regions substantially coplanar with the surface" of the substrate.

<u>Rejections under 35 U.S.C. 103(a):</u> Claims 2-4, 13-14, 16-18, 21-26, 28-29, 32-36, 45 and 46 as being unpatentable over Oyuang in view of Dawson.

<u>Regarding claims 2 and 16</u>

Applicant (pages 16-20 of remark) argues that neither Ouyang nor Dawson teach all limitations recited in claims 2, 13-14, 16, 18, 21-26 and 45.

It is noted that the rejection of above claims is not based on anticipation, but rather, is based on obviousness. Therefore, Applicant's argument has no immediate

apparent relevance to the issues presented by the rejection since Applicant cannot show nonobviousness by attacking references individually where the rejection is based upon a combination of references. _In re Young_, 403 F. 2d 754, 757, 159 USPQ 725, 728 (CCPA 1968). The examiner relies on the combined teachings of Ouyang and Dawson. Dawson is not relied on for teaching the NMOS and PMOS devices having source/drain regions located partially in the substrate or the NMOS source/drain regions having magnitudes of stresses being different from the magnitudes of stresses of the PMOS source/drain regions. Ouyang (Fig. 4B) clearly discloses the NMOS and PMOS devices having source/drain regions located partially in the substrate, and the NMOS source/drain regions having magnitudes of stresses being different from the magnitudes of stresses of the PMOS source/drain regions (par. [0027]). Dawson is relied on for showing that it was known to form a PMOS gate having a height greater than a height of an NMOS gate (see Fig. 1H and column 7, lines 4-6) for the purpose of reducing boron penetration into active region (column 4, lines 32-33). Therefore, Dawson clearly suggests the motivation for combining the references and the combination of Ouyang and Dawson does teach <u>all</u> the limitations recited in the invention as claimed. The examiner thus regards Applicant's assertions as constituting evidence that Applicant has failed to consider as a whole the prior art teachings disclosed by the combining of the references.

Applicant (pages 21-23 of remark) argues that neither Ouyang not Dawson teach all limitations recited in claims 3-4, 17, 28-29, 32-36 and 46.

It is again noted that the rejection of above claims is not based on anticipation, but rather, is based on obviousness. Therefore, Applicant's argument has no immediate apparent relevance to the issues presented by the rejection since Applicant cannot show nonobviousness by attacking references individually where the rejection is based upon a combination of references. *In re Young*, 403 F. 2d 754, 757, 159 USPQ 725, 728 (CCPA 1968). The examiner relies on the combined teachings of Ouyang and Dawson. Dawson is not relied on for teaching the NMOS and PMOS devices having source/drain regions located partially in the substrate or the NMOS source/drain regions having magnitudes of stresses being different from the magnitudes of stresses of the PMOS source/drain regions. Ouyang (Fig. 4B) clearly discloses the NMOS and PMOS devices having source/drain regions located partially in the substrate, and the NMOS source/drain regions having magnitudes of stresses being different from the magnitudes of stresses of the PMOS source/drain regions (par. [0027]). Dawson is relied on for showing that it was known to form the spacers on opposing sides of the PMOS gate having a width greater than a width of the spacers on opposing sides of the NMOS gate because the relative wide spacers for the PMOS device would offset the rapid diffusion of boron in the source/drain regions for the P-channel device during high temperature processing so that the source/drain regions for the NMOS and PMOS devices would have the desired sizes (see Fig. 1H and column 4, lines 32-40). Therefore, Dawson clearly suggests the motivation for combining the references, and the combination of Ouyang and Dawson does teach all the limitations recited in the invention as claimed. The Examiner again regards Applicant's assertions as constituting evidence that

Applicant has failed to considered as a whole the prior art teachings disclosed by the combining the references.

Rejections under 35 U.S.C. 103(a): Claims 38, 39 and 42 as being unpatentable over Ouyang in view of Yeo.

Applicant)pages 23-25) argues that neither Ouyang nor Yeo teach all the limitations recited in claims above.

It is again noted that the rejection of above claims is not based on anticipation, but rather, is based on obviousness. Therefore, Applicant's arguments are not persuasive because what Applicant argues is not shown by one reference is clearly taught by the other. Thus, these arguments are arguments against the references individually but, clearly, these are not proper arguments where references are applied in combination. *In re Keller*, 642 F. 2d 413, 425, 208 USPQ 871, 881 (CCPA 1981). The examiner relies on the combined teachings of Ouyang and Yeo. Yeo is not relied on for teachings each of the NMOS and PMOS devices located partially within the substrate surface or the PMOS device having source/drain regions comprising SiGe. Ouyang (Fig. 4B) clearly discloses each of the NMOS and PMOS devices located partially within the substrate surface and the PMOS device having source/drain regions 10 comprising SiGe (par. [0040]). Yeo is relied on for showing that it was known to form the NMOS device having source/drain regions comprising SiC for the purpose of enhancing significantly the electron mobility of the drive current in the strained channel region (par. [0033], last 8 lines). Therefore, Yeo clearly suggests the motivation for combining the

references and the combination of Ouyang and Yeo does teach <u>all</u> the limitations recited in the invention as claimed.

<u>Rejections under 35 U.S.C. 103(a)</u>: Claim 47 as being unpatentable over Ouyang in view of Okumura.

Applicant (pages 25-27 of remark) argues that Ouyang's Fig. 4B does not suggest that a PMOS includes "source/drain regions recessed within the surface", and an NMOS includes "source/drain regions substantially coplanar with the surface" as claimed.

This argument is not persuasive because Ouyang's Fig. 4B clearly discloses <u>all</u> the limitations recited above. The previous discussions of Ouyang's Fig. 4B regarding to claim 1 rejection above are incorporated herein for reference.

<u>Rejections under 35 U.S.C. 103(a):</u>

A. Claims 27 and 37 as being unpatentable over Ouyang in view of Dawson and Shimizu.

B. Claim 43 as being unpatentable over Ouyang in view of Yeo and Shimizu.

Applicant (pages 27-31) argues that neither the combination of Ouyang, Dawson and Shimizu nor the combination of Ouyang, Yeo and Shimizu disclose all the limitations as claimed.

These arguments are not persuasive because as previously discussed in details above, the combination of Ouyang and Dawson or the combination of Ouyang and Yeo substantially suggests the invention as claimed. Furthermore, because Shimizu clearly teaches the forming of an etch stop layer over a CMOS device for imparting the different

stresses in the source/drain regions and for improving the drive currents for both NMOS and PMOS devices (see abstract), one skilled in the art would motivate to combine the reference as suggested.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
March 17, 2006

PHAT X. CAO
PRIMARY EXAMINER